AMENDMENT TO THE SPECIFICATION

Please amend Paragraphs [0013]-[0014] on page 4 as follows:

[0013] Referring to FIG. 1, a block diagram of a system [[10]] for scrambling/descrambling data in parallel is illustrated. A storage means 20 contains a subset of a receiving sequence of scramble bits to be used in scrambling data in parallel. The contents of the storage means 20 is sent to both a predict logic block and a scramble logic block. Both these logic blocks 30, 40 are combinational circuits which perform operations using the contents of the storage means 20. The scramble logic block 40 also receives the input data 50 in parallel.

[0014] It should be noted that scrambling/descrambling operations, especially for self-synchronous scrambling/descrambling systems, are essentially sequential or serial in nature. The current state of the scrambler/descrambler determines its immediate future state. However, this very feature leads to scrambling/descrambling bit sequences that are periodic or that repeat every set number of iterations. The system [[10]] for scrambling/descrambling data in parallel works by taking advantage of this periodic or recurring nature of most scrambling bit sequences. By treating the scrambling bit sequence as a counter whose status/state can be predicted based on the current values, the bits required for scrambling further input bits can be predicted and generated. As an example, if $SCR[0]_n$-$SCR[6]_n$ are taken as the bit states of bits 0 to 6 of a 7 bit scrambling sequence at iteration n, then these values are used in scrambling single bit input data $IN[0]_n$. For serial operation, $SCR\ [0]_{n+1}$-$SCR\ [6]_{n+1}$ are then used to scramble input data $IN[0]_{n+1}$ with $SCR[0]_{n+1}$- $SCR[6]_{n+1}$ being generated from $SCR[0]_n$ - $SCR[6]_n$ only.